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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,865	09/30/2003	Seok-Jun Won	9898-305	7630
7590 12/01/2004			EXAMINER	
MARGER JOHNSON & McCOLLOM, P.C. 1030 S.W. Morrison Street Portland, OR 97205			LOKE, STEVEN HO YIN	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/676,865	Applicant(s) WON, SEOK-JUN	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 12-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 9 and 10 is/are rejected.
- 7) ☒ Claim(s) 7, 8 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/30/03</u> . | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2811

1. Applicant's election without traverse of claims 1-11 in the reply filed on 10/12/04 is acknowledged.
2. Claims 12-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10/12/04.
3. Claims 4 and 10 are objected to because of the following informalities: Claim 4, lines 2-3, claim 10, lines 2-3, the phrases "BST", "PZT", and "ST" should be in full written form instead of in abbreviation. Appropriate correction is required.
4. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, line 9, the phrase "the upper interconnection" is unclear whether it is being referred to the first upper interconnection.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4 insofar, as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Nakajima et al.

In regards to claim 1, Nakajima et al. show all the elements of the claimed invention in fig. 1. It is a flat-type capacitor, comprising: a lower interconnection [8a] on a predetermined portion of a semiconductor substrate [1]; a lower electrode [24] that is electrically coupled to the lower interconnection [8a]; a concave dielectric layer [25b] formed on the lower electrode [24]; a concave upper electrode [26] formed on the dielectric layer [25b], wherein the concave upper electrode [25b] is larger than the lower electrode [24]; a first upper interconnection [21] being electrically coupled to the lower interconnection [8a]; and a second upper interconnection [16A] that is coupled to the upper interconnection [21] when the memory cell transistor is in the on-state.

In regards to claim 2, Nakajima et al. further disclose the lower electrode [24] is positioned between edges of the concave upper electrode [26].

In regards to claim 3, Nakajima et al. further disclose the lower electrode [24] and the upper electrode [26] are composed of TiN.

In regards to claim 4, Nakajima et al. further disclose the dielectric layer [25b] is composed of Ta₂O₅.

7. Claims 5, 6, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regards to claim 5, Kim et al. show all the elements of the claimed invention in fig. 9. It is a flat-type capacitor, comprising: a first metal interconnection [124] formed on a predetermined surface of a semiconductor substrate [102]; a first interlayer dielectric (a lower portion of layer [120]) formed on the first metal interconnection [124] and the semiconductor substrate [102]; a second interlayer dielectric (an upper portion of layer [120] that has a thickness similar to the thickness of layer [130]) formed on the first interlayer dielectric [120]; a lower electrode [130] formed on the first interlayer dielectric [120] and coupled to one side of the first metal interconnection [124]; a second metal interconnection (a portion of layer [124] in contact [126b] that has the same thickness as the second interlayer dielectric) formed on the first interlayer dielectric [120] and electrically isolated from the lower electrode [130] when the memory cell transistor in the off-state; a third interlayer dielectric [128] formed on the second interlayer dielectric; a concave dielectric layer [132] formed on the lower electrode [130] and the second interlayer dielectric; a concave upper electrode [134a] formed along a top surface of the concave dielectric layer [132], wherein the concave upper electrode [134a] is larger than the lower electrode [130]; a fourth interlayer dielectric [140] formed on the concave dielectric layer [132], the concave upper electrode [134a], and the third interlayer dielectric; and a plurality of third metal interconnections [148] formed on the fourth interlayer dielectric [140], wherein one of the third metal interconnections [148] is

coupled to the upper electrode [134a] and another one of the third metal interconnections [148] is coupled to the second metal interconnection [124].

In regards to claim 6, Kim et al. further disclose the lower electrode [130] is positioned between edges of the concave upper electrode [134a].

In regards to claim 9, Kim et al. further disclose the lower electrode, the second metal interconnection, and the second interlayer dielectric have the same thickness.

In regards to claim 10, Kim et al. further disclose the dielectric layer [132] comprises SiO₂.

8. Applicant cannot rely upon the foreign priority paper to overcome the rejection in paragraph 7 because a translation of said paper has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

9. Claims 7, 8 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is the upper electrode and the second metal interconnection are formed of the same material. The second major difference in the claims not found in the prior art of record is the first, second, third, and fourth interlayer dielectrics have the same etch selectivity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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November 29, 2004

Steven Loke
Primary Examiner

